

Semiconductor Traceability and Provenance Workshop

A NIST Workshop

Melissa Grupen-Shemansky, PhD / CTO & VP Technology Coalitions / January 27, 2026

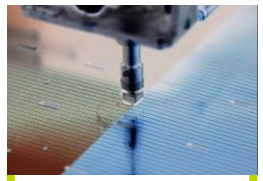
SEMI Connects the $3.0T+ Global Electronics Design and Manufacturing Supply Chain

SEMI OVERVIEW

From Chip Design to Electronics Systems



Design Automation
$15B



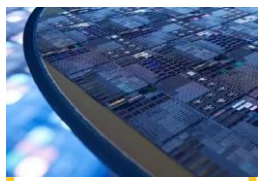
Materials
$72B
Subassemblies Components
$18B



Total Equipment
$107B



Assembly & Test Services
$40B



Semiconductors
$580B



Electronic Systems
$2.5T

SEMI

Smart Initiatives

SMART DATA-AI

SMART MANUFACTURING

SMART MEDTECH

SMART MOBILITY

Technology Communities

ESDA Electronic System Design Alliance

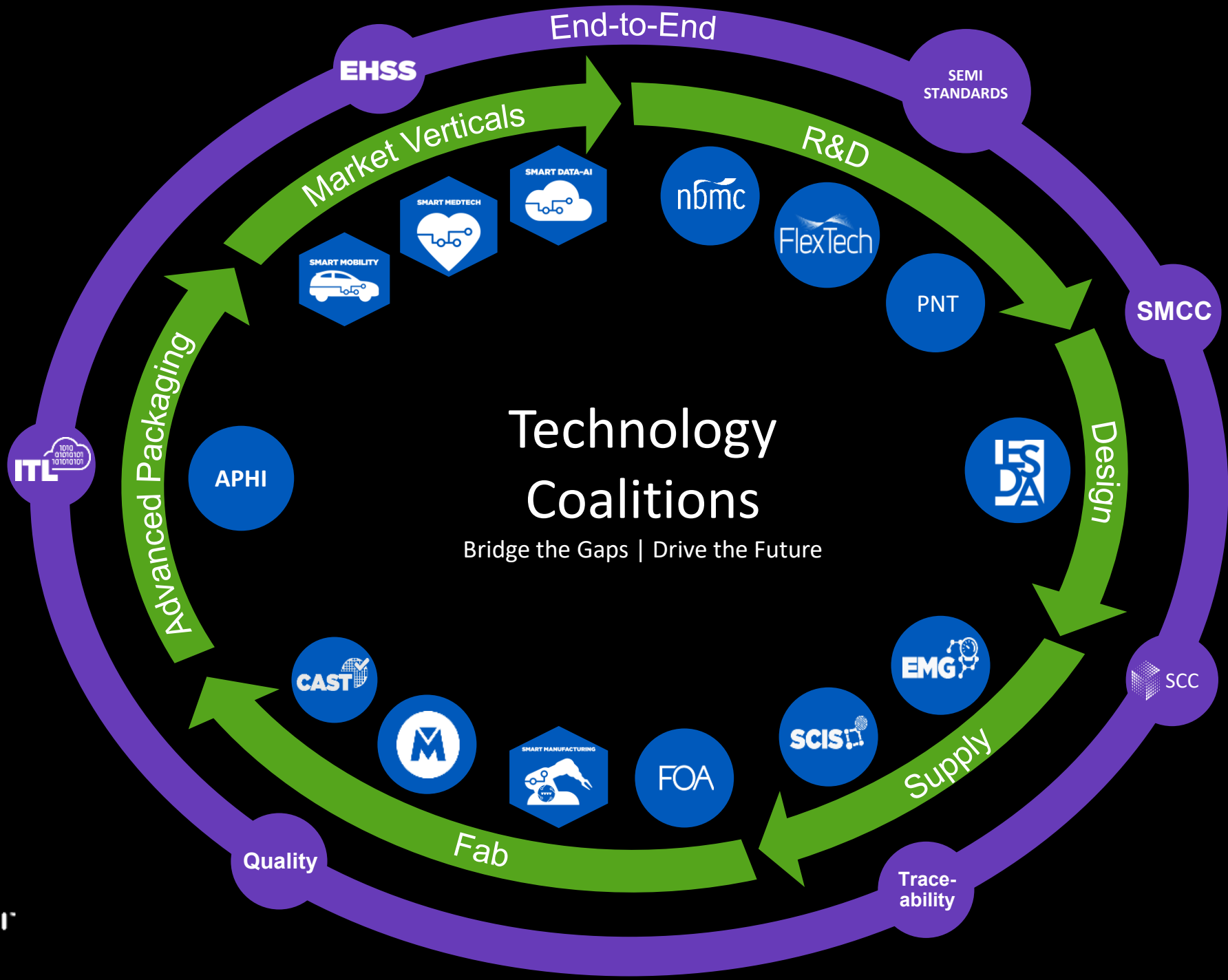
FOA fab owners alliance

FlexTech

MEMS & SENSORS INDUSTRY GROUP

SOI industry consortium

2023 Market Data Estimates Sources: SEMI, IC Insights and TechInsights

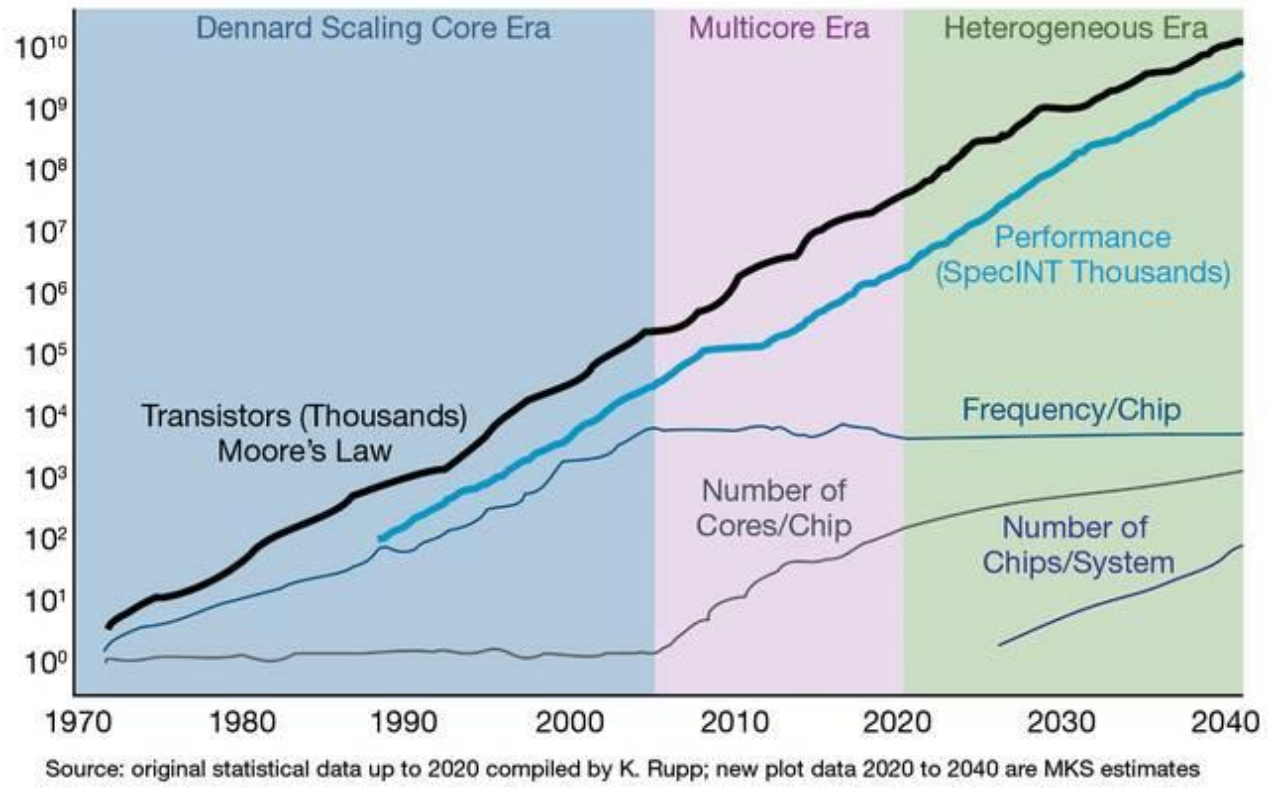

End-to-End
EHSS
SEMI STANDARDS
SMCC
SCC
Trace-ability
Quality
ITL
APHI
Market Verticals
SMART DATA-AI
SMART MEDTECH
SMART MOBILITY
R&D
nbmc
FlexTech
PNT
Design
ESDA
Supply
EMG
SCIS
FOA
SMART MANUFACTURING
Fab
CAST
Advanced Packaging
Technology Coalitions
Bridge the Gaps | Drive the Future

“ The semiconductor race is no longer just a technological competition — it has become a strategic fault line in the global balance of power ”

From the report titled “Silicon Under Siege: The Cyber War Reshaping the Global Semiconductor Industry”

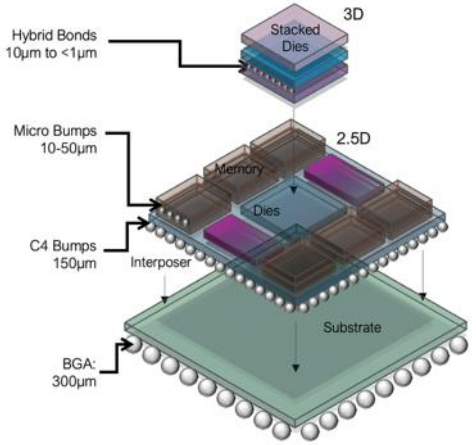


Birth of the Heterogeneous Multi-die Era



Source: original statistical data up to 2020 compiled by K. Rupp; new plot data 2020 to 2040 are MKS estimates

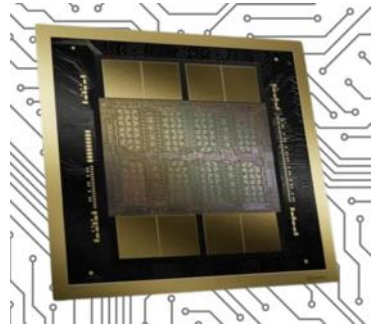
Birth of "Chiplets" and 2.5D and 3D Array Assembly



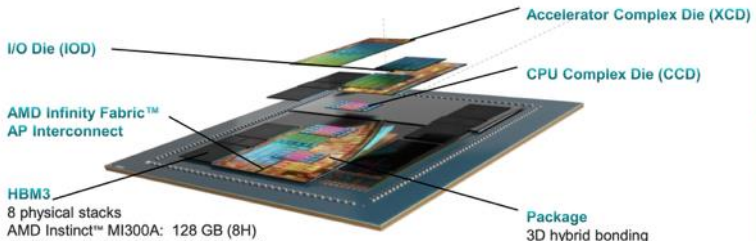
Nvidia Blackwell™

2024

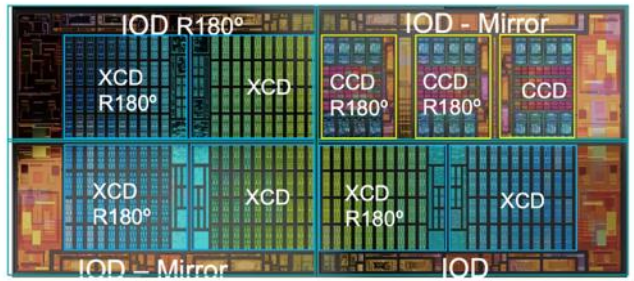
104B Transistors
4nm Process Node – TSMC 4NP
Hit the Silicon Reticle Limit so
2 Blackwell Die are packaged together in the final array for a total of 208B Transistors



AMD Instinct™ MI300.



(a) MI300 Die information



(b) MI300 modular architecture

2023

146B Transistors for M1300A
153B Transistors for M1300X
5 & 6nm Process Nodes

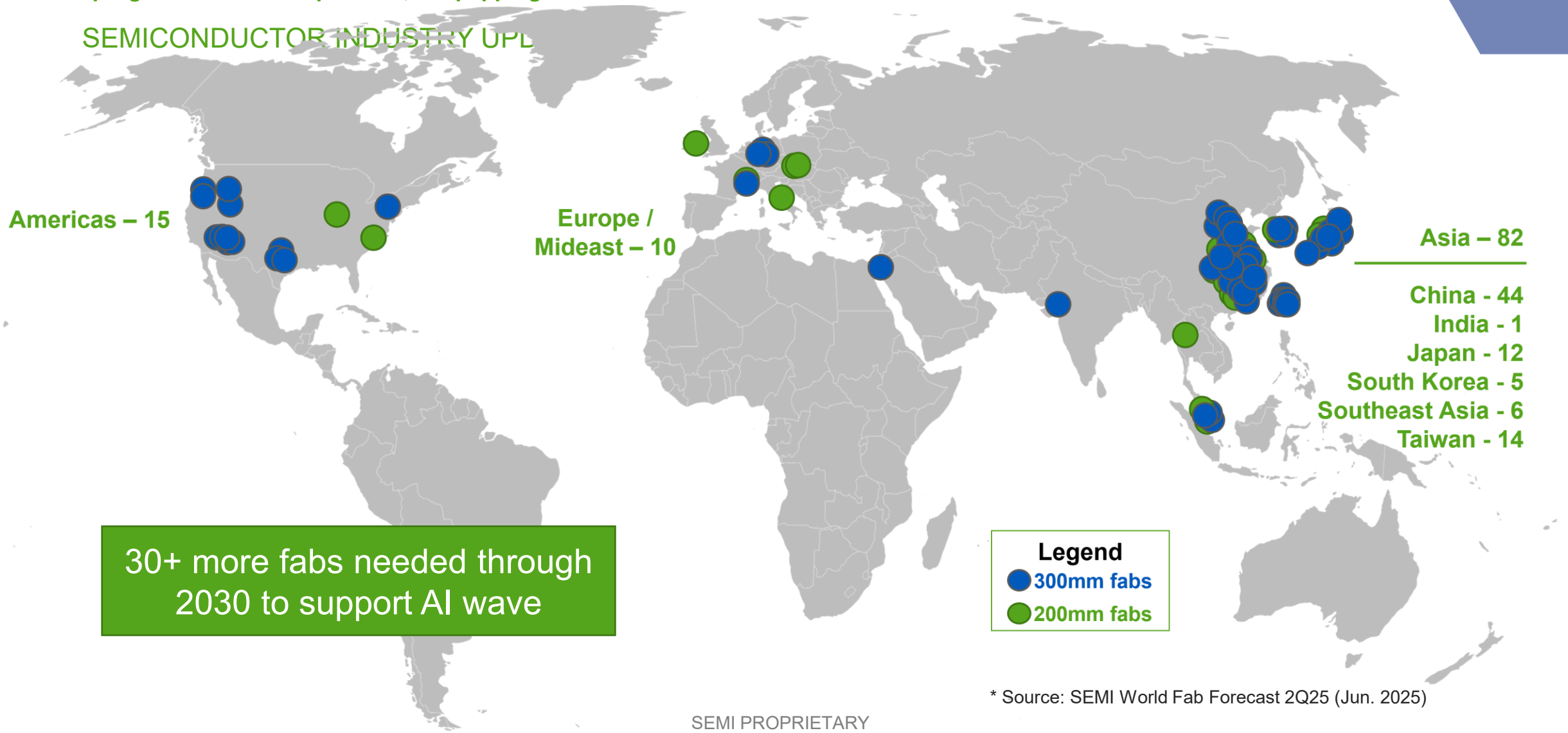
Slide Credit: Reed Hinkel, Synopsys

Unprecedented Fab Expansions to Realize $1T

107 300mm and 200mm New Fabs Coming Online Between 2024-2028*

- **91 in progress with 48 in operation, 9 equipping and 34 under construction**

SEMICONDUCTOR INDUSTRY UPL



30+ more fabs needed through 2030 to support AI wave

* Source: SEMI World Fab Forecast 2Q25 (Jun. 2025)

SEMI New Initiatives: Traceability

Idea Screen › 2nd Screen › Development › Go to Test › Launch › Optimize Pivot

Idea Generation

Stage 0: Scoping
1. Assemble Team
2. Define Motivation
3. Scope 1.0
4. Benchmark and Risks

Stage 1: Spec and Plan

Stage 2 : Design and Development

Stage 3: Testing & Validation

Stage 4: Launch

Gate 0: Discovery Complete Industry need and market priority proposed

Gate 1: Demonstrated Initiative Demand Market Research, Industry Driver Member Feedback, Stakeholder Input (Advisory, Core Industry Team Review/Approval)

Gate 2: Demonstrated Initiative Viability Product Reqs, Business Case, Marketing & Sales, Launch Plans (Advisory - Industry Team Revie - Approval)

Gate 3: Initiative Developed Execution of Initiative Requirements and Dev & Launch Plans (Advisory, Industry Team Review and Approval)

Gate 4: Market Acceptance/ Validation Completed Near, Field, and Market Testing (Advisory – Industry Team Review and Approval)

Post Launch Review (Advisory – Industry Team)

Phase 0 Checklist

Checklist needed for each phase and Go/No Go decision at each gate.

- **Gate 0 ‘GO’ criteria: committed resources (human and financial)**
- **Identify supply chain stakeholders and assemble core industry team**
- **Motivation statement / industry driver / strategic significance to industry (prioritization tools)**
- **Scope**
  - **Capitalize on common goals within other SEMI initiatives**
- **Objectives & deliverables – high level, first pass**
- **Initial Timeline or Schedule**
- **Cost analysis including resources necessary for next phases**
- **Benchmark and existing solutions**
- **Risk analysis**

MOTIVATION

Motivation – Input from EDA, IDMs, Fabs, & Fabless

Question: What benefits can an industry wide scalable traceability system offer?

Supply Chain Visibility & Assurance

- Ensures accurate provenance of materials and genuine silicon
- Provides real-time, reliable information about any object in the supply chain.
- Enables consistent, interoperable data sharing across participants legitimizing data for high integrity AI, enhanced supply chain visibility, and supplier validation

Lifecycle Management and Sustainability

- Enables lifecycle tracking for reuse, recycling, and end-of-life management
- Improves monitoring of product reliability over time
- Can minimize error-prone human intervention improving efficiency, mitigate security vulnerabilities, and enhance forensics

Compliance and Governance

- Aligns industry with accepted standards and may support geo-regulatory and export control compliance

Competitive Advantage

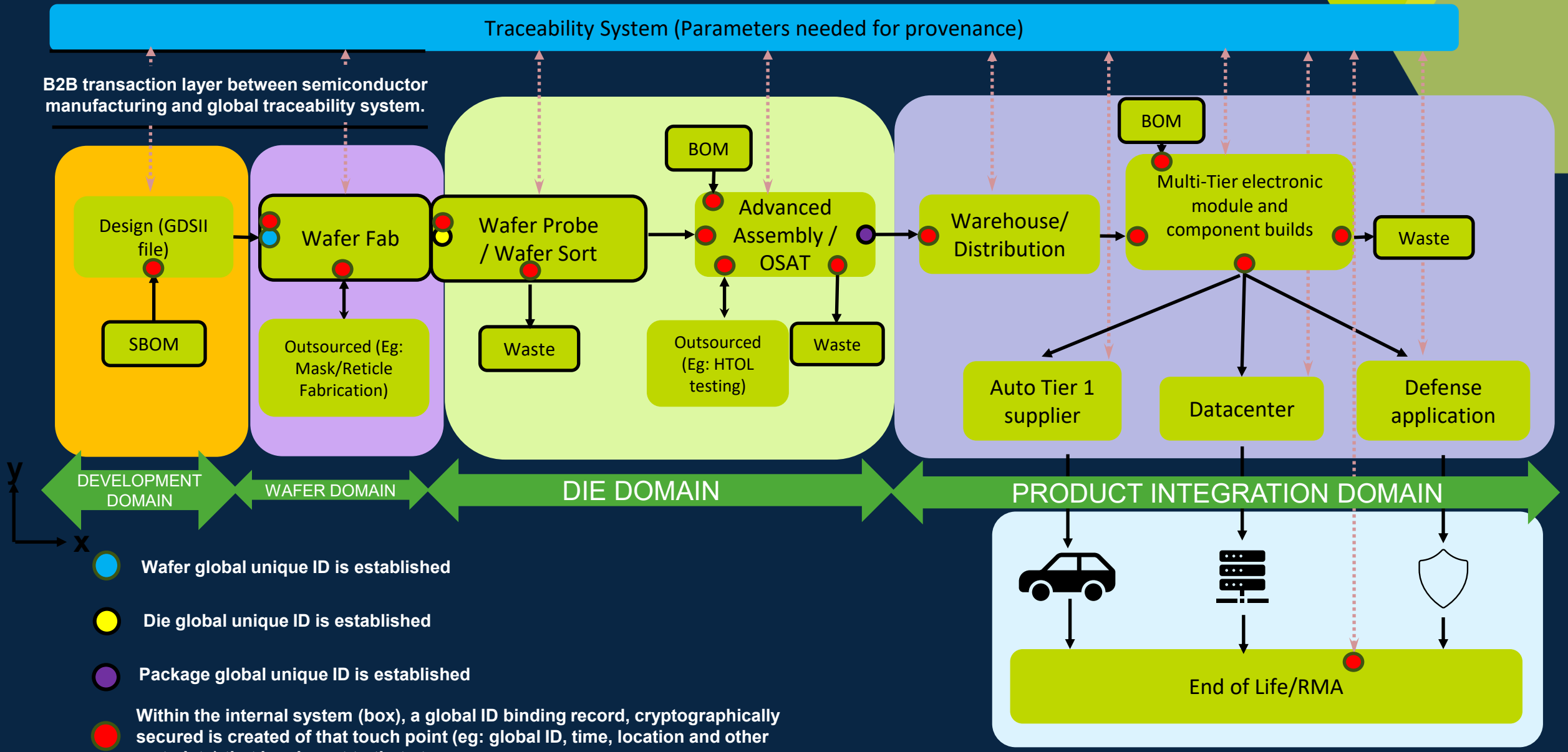
- Stay ahead of non-participants of the traceability system
- Reinforces credibility through trusted parity among ecosystem members



semi

SCOPE

SEMI Phase 0 Chip Traceability: Journey from design to application



Wafer global unique ID is established

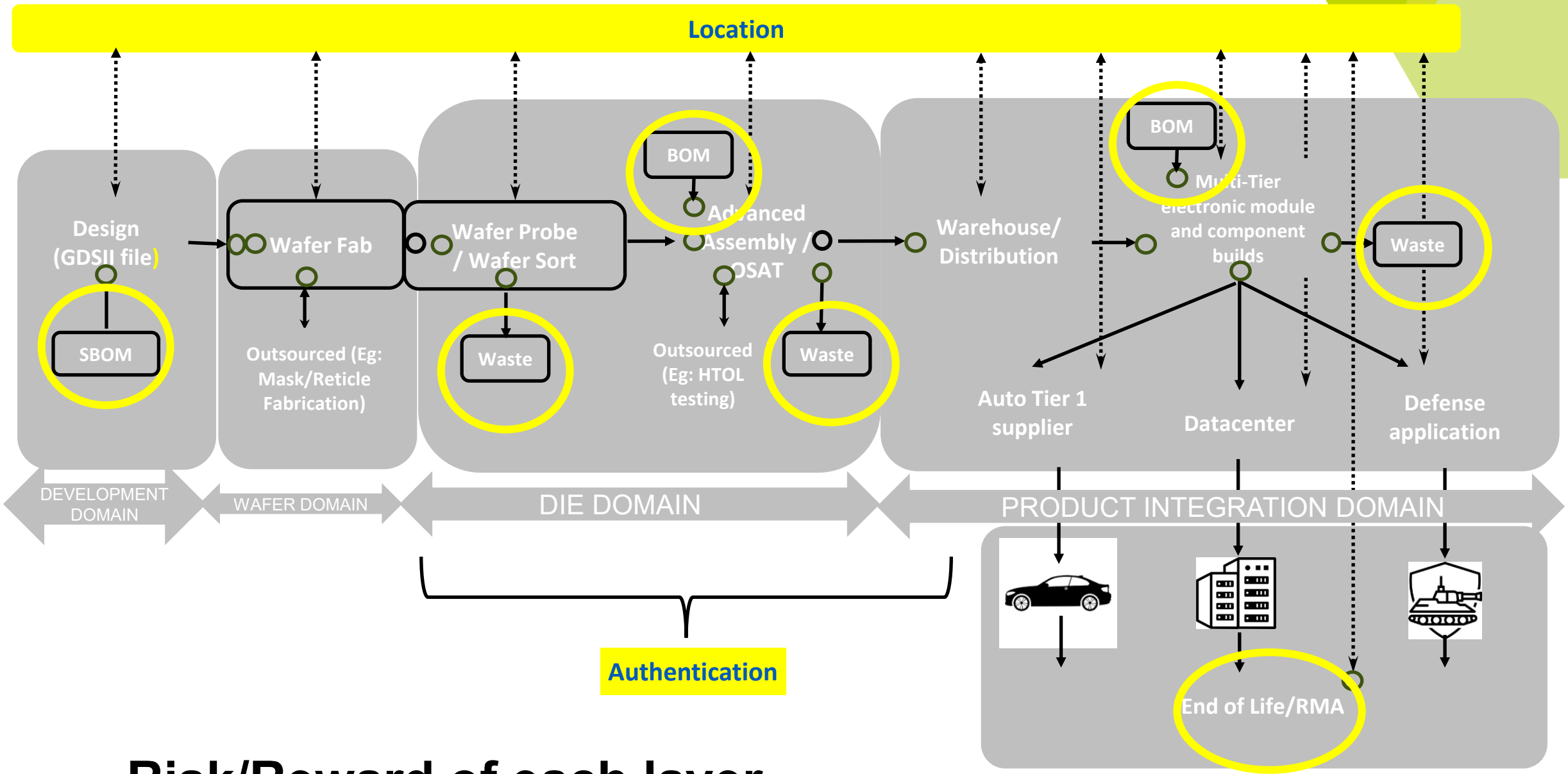
Die global unique ID is established

Package global unique ID is established

Within the internal system (box), a global ID binding record, cryptographically secured is created of that touch point (eg: global ID, time, location and other metadata) that is relevant to that step

3 levels of security needed

SEMI Phase 0 Chip Traceability: Journey from design to application



Risk/Reward of each layer

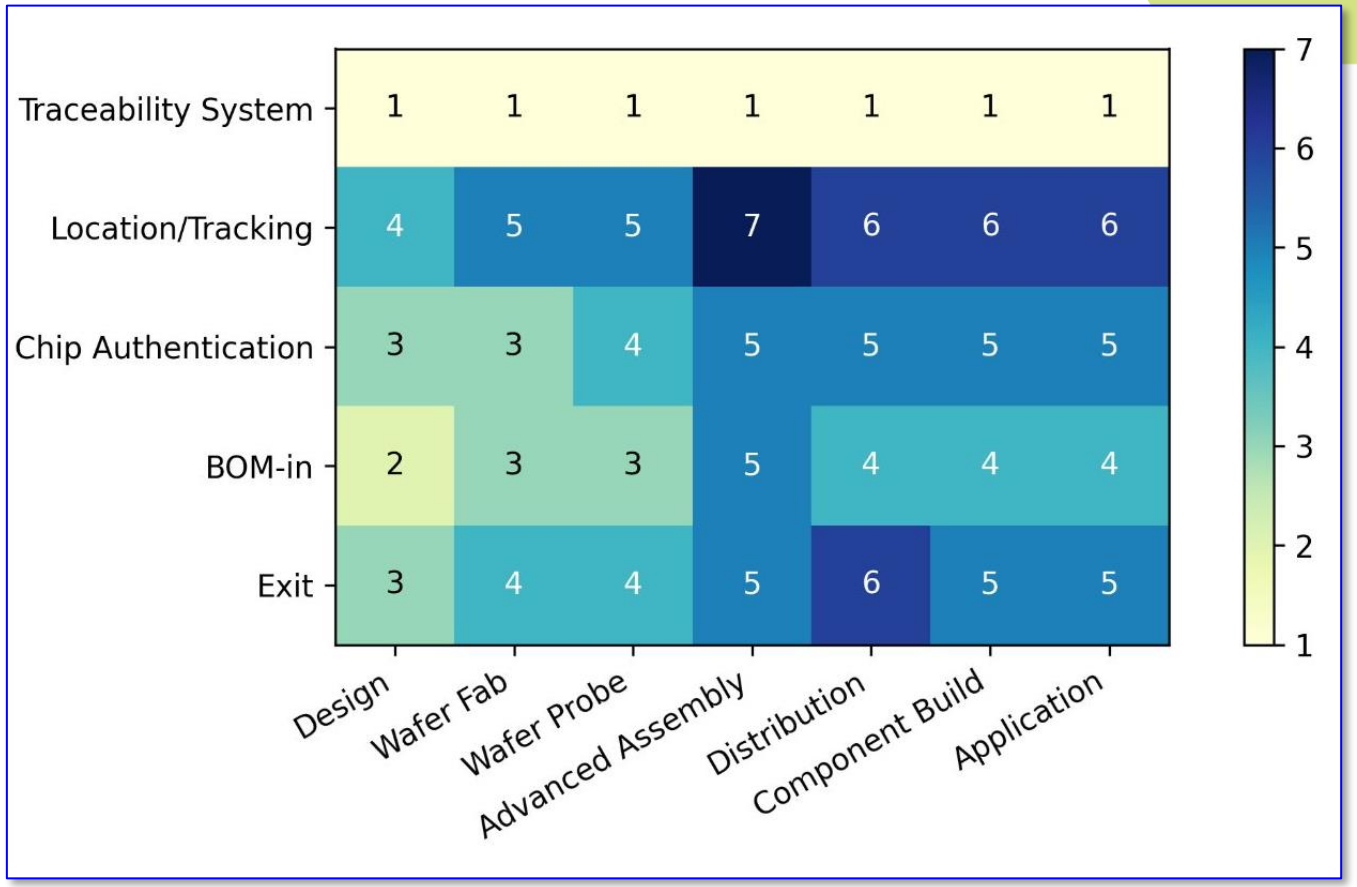
3 levels of security needed

Phase 0 Results

Traceability Capability Analysis

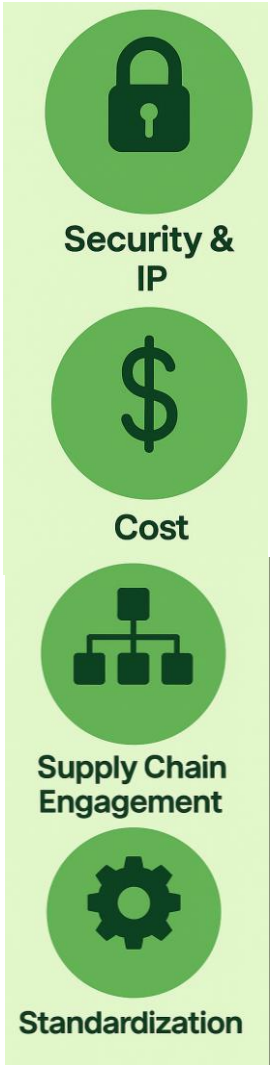
Solution providers including IP, EDA, and IT companies

- **Traceability System**
  - A global system where traceability information is recorded and persisted
  - Represents one start-up that has not implemented in semiconductor sector
- **Location or Tracking**
  - Serialized global unique ID with location stamp and cataloging system
  - Companies D, E, G appear frequently, suggesting strong traceability offerings
- **Chip Authentication**
  - Encrypted key or PUF-based chip authentication
  - Numerous device design companies have authentication technologies that are considered proprietary – not represented here
- **BOM in (Software/Hardware)**
  - Includes design IP blocks
- **Exit (Waste/RMA)**
  - Chips or assemblies are removed from the tracking flow as binned, scrap or EOL



Risk Analysis Results

Input from EDA, IDMs, Fabs, Fabless, & Solution Providers



Security and IP

- Risk of exposing sensitive or proprietary data during traceability processes and the inherent vulnerabilities from the traceability system.

Transparency vs. Confidentiality

- Balancing openness with the need to obfuscate proprietary data.

Data Integrity Issues

- Potential for wrong or misleading information about objects, impacting trust.

Full Supply Chain Engagement

- Difficulty in achieving compliance and participation across all tiers globally including industry and government stakeholders.
- Building a democratized, standardized framework across geographies is complex.

Cost Implications

- High infrastructure costs and unclear cost-benefit ratio for implementation.

Standardization Issues

- Lack of unified standards and governance, including no common traceability infrastructure, unclear ownership of a central record and difficulty integrating legacy devices and smaller suppliers.

Example Industry Standards on Traceability (Noncomprehensive)

Item	Standard	Description
1	**JEDEC – JEP30**	Defines a standardized digital part model that enables consistent, machine-readable component data exchange, to reduce errors and ensure accurate, structured information sharing between manufacturers and customers.
2	**GS1 Standards**	A global, interoperable framework that enables organizations to uniquely identify products, capture key supply chain events, and share traceability data across partners using a common language. It includes Identification Standards (Global Unique IDs), Data capture standards (Barcodes and Data Carriers) and Data sharing Standards.
3	**IPC- 1782**	Manufacturing and supply-chain traceability standard that defines minimum, risk-based requirements for tracking electronic components, materials, and processes to prevent counterfeits, support root-cause analysis, and ensure product integrity across internal and external operations.
4	**ISO9001:2015**	Requires organizations to identify and control products/services when necessary for conformity, maintaining records (documented information) to enable tracing outputs to their origins (materials, processes, people) and status (monitoring/measurement) throughout production using unique identifiers and documented evidence for full traceability from raw materials to finished goods. (Clause 8.5.2)
5	**NIST**	NIST IR 8419: Blockchain and Related Technologies to Support Manufacturing Supply Chain Traceability: Needs and Industry Perspectives NIST IR 8536: (Draft Document): Supply Chain Traceability: Manufacturing Meta-Framework: Presents a framework to improve traceability across complex and distributed manufacturing ecosystems. It enables structured recording, linking, and querying of traceability data across trusted repositories.
6	**SEMI T27**	Traceability Identification Label of Component Parts: Standardize the design of the ID label for use in establishing a system of transferring the traceability information in an efficient and timely manner between the user and the supplier.

SEMI Phase 0 Existing Traceability Solutions (partial list)

Item	Company	Description
1	**Rambus**	Provides silicon-proven Root of Trust IP, which embeds 3 things: (a) a secure device ID, (2) cryptographic keys (private key value), and (3) a signed certificate directly into a PUF on the chip.
2	**Synopsys**	System that manages SRAM PUF Keys - a PUF that used process variations to create a unique silicon fingerprint (unique device ID)
3	**PDF Solutions**	PDF provides traceability that links to manufacturing data to improve reliability without requiring a specific physical identifier. All devices are traced which is especially important with the trend toward complex chip-let packaging
4	**Hushmesh**	Security starts with secure servers (secure web) - and verified chips. Any provenance and traceability system can only be as trustworthy as the provenance and traceability of all underlying keys and cryptographic implementations.
5	**GS1**	Create Standards including those for traceability and provide support to implement the standards. Their traceability standard has been adopted in the US and Europe used in the Pharma Industry.
6	**Caliptra (AMD, Google, Microsoft, Nvidia)**	Caliptra is an open-source Silicon Root of Trust (RoT) integrated into SoCs that provides identity, measurement, attestation, and secure ownership transfer, all of which form the cryptographic backbone required for end-to-end semiconductor traceability.

Proposed next steps – Phase 1

- Examine, adopt, or modify present standards and frameworks
  - For example, GS1 has national data bases in 117 countries, excellent for identifying companies and locations, but presently incapable of handling the volume of part numbers within the semiconductor industry – part #’s in the trillions.
- Resource exemplar product traceability proof of concept
  - Full supply chain participation and collaboration required
  - Federal stakeholder participation necessary to address national goals
- Execution plan for scale and resilience
  - Including vulnerabilities analysis for IP and National Security

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THANK YOU

